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A Survey of Different Barrier layers and Indium Content of InGaAs MOSFETs

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***Abstract*— A barrier layer in an InGaAs MOSFET, which shows promise for high-performance logic applications due to enhanced electron mobility, is known to further improve the electron mobility. In this paper, a detailed investigation of the impact of different barrier layers on the analog performance of an InGaAs MOSFET is reported for the first time. The device parameters for analog applications, such as transconductance (g_m), transconductance-to-drive current ratio (g_m/I_{DS}), drain conductance (g_d), intrinsic gain (g_m/g_d), and unity-gain cutoff frequency (f_T) are studied with the help of a device simulator. A barrier layer is found to improve the analog performance of such a device in general; with a double-barrier layer showing the best performance. An investigation on the impact of varying the indium content in the channel on the analog performance of an InGaAs MOSFET with a double-barrier layer is also reported in this paper. It is found that a higher In content results in better analog performance of such devices.**

***Index Terms*— Buried-channel InGaAs MOSFET, device gain, indium content, transconductance, unity-gain cutoff frequency.**

I. Introduction

Recently, InGaAs-channel MOSFETs have attracted a lot of interest amongst the researchers for high-performance logic applications due to its enhanced electron mobility [1]–[3]. Recent investigations reveal that the buried-channel InGaAs MOSFETs can achieve much higher effective electron mobility (>5000 $cm^2/V.s$) [2] than that in the surface channel devices, in which the effective electron mobility is usually less than 2000 $cm^2/V.s$. On the other hand, a barrier layer reduces the gate control over the channel. As a result, surface-channel devices, as compared with the buried-channel devices, exhibit lower subthreshold swing and better immunity to short-channel effects (SCEs), such as drain-induced barrier lowering (DIBL) [3]. It is reported [4] that incorporation of higher mole fraction of indium in the channel further enhances the electron mobility.

The development of lattice mismatched InAlAs/InGaAs high electron mobility transistors on high-quality GaAs substrates (metamorphic HEMT) is of primary interest for millimeter-wave devices. These heterostructures grown on lattice mismatched substrates allow an extension of the composition range in the structures and to exploit enhanced properties, provided that the crystalline perfection of the layers as well as electrical quality are preserved. The aim of this work is to study the influence of indium mole fraction on material properties as well as its consequences on device performance.

In the past one decade or so, the analog performance of the scaled CMOS devices has also received considerable attention particularly for mixed-signal system-on-chip (SoC) applications where the analog circuits are realized together with the digital circuits and memories in the same integrated circuit in order to reduce the cost and improve the performance. In this paper, we report, for the first time, an investigation of the impact of different barrier layers on the analog performance of an InGaAs MOSFET. The analog performance of such a device with a channel length of 40 nm is investigated in terms of transconductance (g_m), output conductance (g_d), intrinsic voltage gain (g_m/g_d), transconductance-to-drain current ratio (g_m/I_{DS}), and the unity-gain cutoff frequency (f_T). We also report an investigation of the impact of varying the indium content of the channel on the analog performance of an InGaAs MOSFET with a double-barrier layer.

II. Device Structure and Simulation

The cross-sections of n-channel InGaAs MOSFETs of chan-nel length 40 nm, with no barrier, a single barrier, and a double barrier are shown in Fig. 1(a)–(c), respectively. The details of the process flow for the fabrication of such a device are reported in [3]. Three different configurations of the channel are used in this paper: 1) with no barrier layer (i.e., surface-channel device); 2) with a single-barrier layer consisting of a 1-nm InP layer; and 3) with a double-barrier layer consisting of 1.5-nm $In_{0.52}Al_{0.48}As$ and 2-nm InP layers. The device structure comprises a 300-nm $In_{0.52}Al_{0.48}As$ buffer layer and a 10-nm quantum well InGaAs. A 20-nm $In_{0.53}Ga_{0.47}As$ cap layer is used for all the devices. All the layers are undoped except the top $In_{0.53}Ga_{0.47}As$ layer, which is heavily doped with n-type impurities intended for the source and the drain. TaN is used as a gate material and Au is used for the formation of ohmic source and drain contacts.

2-D numerical device simulations are done for the InGaAs MOSFET with the above-mentioned three different barrier layers using SILVACO ATLAS [5]. Since InGaAs is an alloy, its dielectric constant is computed using linear interpolation among the corresponding reported parameters of the con-stituents GaAs and InAs [6], [7]. The compressive strain devel-oped in the $In_xGa_{1-x}As$ channel grown using InP substrate and InAlAs buffer is taken into account in the calculation of bandgap values as well as the corresponding conduction and valence band offsets following the technique adopted in [8].

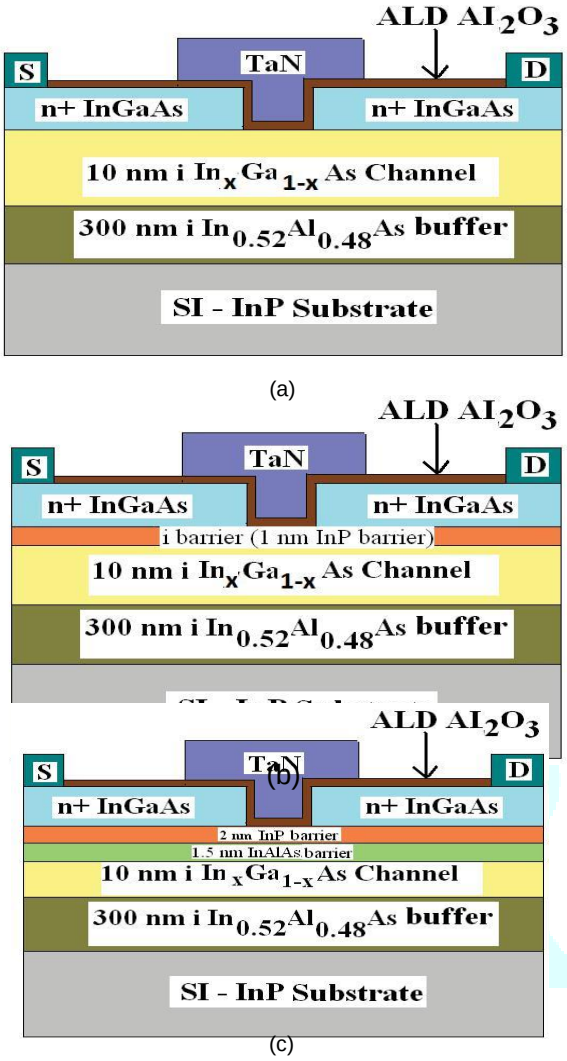


Fig. 1. Schematic device structure of an n-channel InGaAs MOSFET
(a) without a barrier layer, (b) with a barrier layer, and (c) with a double-barrier layer.

TABLE I
BAND OFFSET VALUES BETWEEN DIFFERENT HETEROINTERFACES

Heterointerface	Mole Fraction, x	ΔEc (eV)	ΔEv (eV)
Al2O3/InP	-	4.39	0.96
InP/In0.52 Al0.48As	-	0.26	0.14
$In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$	0.53	0.53	0.18
	0.65	0.70	0.13
	0.70	0.77	0.10
	0.75	0.83	0.08
InP/In_x Ga1−x As	0.53	0.43	0.18
	0.65	0.60	0.13
	0.70	0.66	0.10
	0.75	0.73	0.08
Al2O3/In_x Ga1−x As	0.53	4.55	1.35
	0.65	4.59	1.43
	0.70	4.63	1.44
	0.75	4.66	1.45

dielectric are 6 nm [3] and 6.65 eV [15], respectively. The Pd/Ge source/drain contact resistance used in our studies is 6.66×10^{-8} _cm^2 [16]. Experimental findings reveal that the InGaAs/high-k interface contains appreciable amount of interface trap charge density in the range of 1×10^{12} to 4×10^{12} eV^{-1}cm^{-2} [1]–[3], which is also incorporated in our simulations.

The conduction and valence band offsets between Al2O3 and the InP barrier layer or InGaAs channel are calculated using [5]. The band offset values used for the different heterointerfaces such as insulator/channel, insulator/barrier, and barrier/channel are listed in Table I. Also, the reported values [8]–[10] of the dielectric constant and the band gap of the barrier materials InP and InAlAs are used. The reported experimental results for effective electron mobility at different electric fields are used to extract the simulation parameters, as appeared in the CVT Lombardi model pertaining to the InGaAs channel. Different mobility versus effective electric field and inversion charge density curves for different molar contents of indium in the InGaAs channel as reported in [3], [4], and [11]–[13] are used to extract such model parameters. The work function of TaN gate used in our simulation is 4.5 eV [14]. The thickness and band gap of the Al2O3 gate

III. RESULTS AND DISCUSSIONS

A. Impact of a Barrier Layer

We first make a comparison of the simulated device char-acteristics with the experimental data, as reported in [3], for the In0.7Ga 0.3As n-MOSFETs with the three different structures of the barrier. Such model calibration is shown in Fig. 2(a) and (b) for IDS as a function of gate-to-source voltage VGS at drain-to-source voltage VDS = 50 mV and 0.5 V, respectively. A good agreement between the simulated and experimental characteristics is evident in Fig. 2 for different barrier layers in the device, which ensures the validity of our simulation techniques. Fig. 3 shows the variation of g_m as a function of gate overdrive voltage

V_{GT} (= V_{GS}–V_T , where V_T is the threshold voltage) at V_{DS} = 0.5 V. The value of V_T is extracted as per the constant current definition (10^{-7} A/μm) and found be −0.01, −0.26, and −0.3 V for no barrier, single-barrier, and double-barrier devices, respectively, which are also in consistence with that reported in [3]. Significant improvement in g_m is observed in Fig. 3 for a device with a barrier layer in general; with a double-barrier layer showing the best results. A barrier layer keeps the channel away from the insulator–semiconductor interface. Hence, the channel carriers suffer less amount of scattering thereby enhancing the channel mobility. Consequently, both I_{DS} and g_m show improvement, as evident in Figs. 2 and 3, respectively. On the other hand, incorporation of a barrier layer adds an additional capacitance to the oxide capacitance in series, which in turn decreases the overall capacitance; with maximum reduction in a double-barrier device. Decrease in the overall capacitance due to the use of a barrier layer

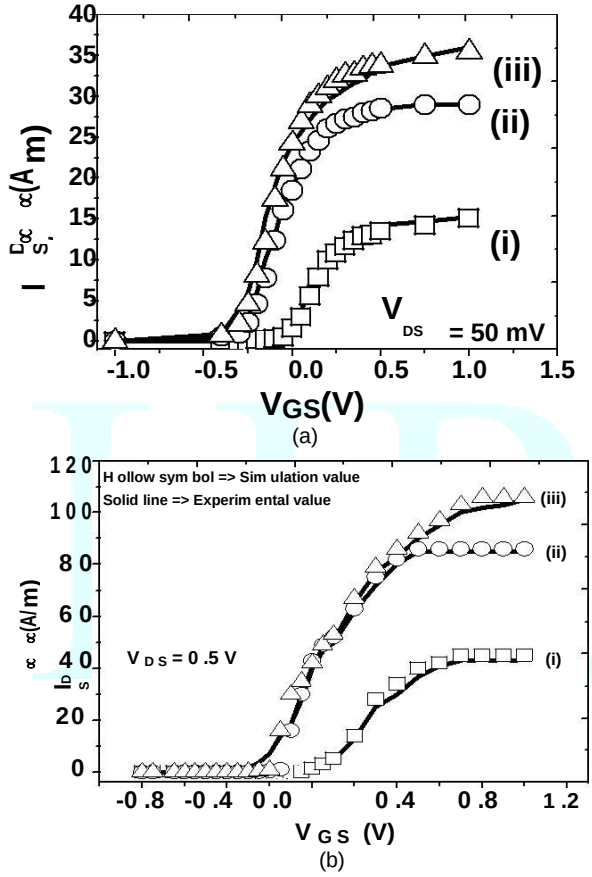


Fig. 2. Comparison of transfer characteristics between the experimental (symbols) and the simulation (lines) results for the $In_{0.7}Ga_{0.3}As$ devices at (a) V_{DS} = 50 mV and (b) V_{DS} = 0.5 V with (i) no barrier, (ii) an InP single barrier, and (iii) an InP/InAlAs double barrier.

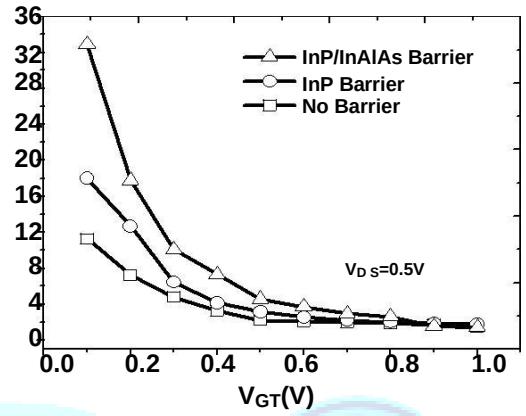


Fig. 4. Comparison of g_m / I_{DS} at V_{DS} = 0.5 V as a function of V_{GT} for the three types of $In_{0.7}Ga_{0.3}As$ MOSFETs.

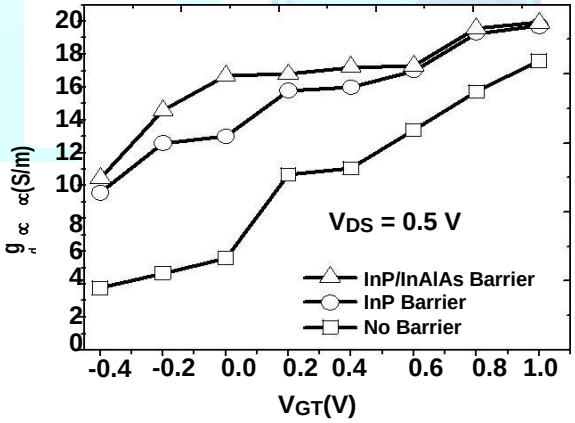


Fig. 5. Comparison of gd V_{DS} = 0.5 V at as a function of V_{GT} for the three types of $In_{0.7}Ga_{0.3}As$ MOSFETs.

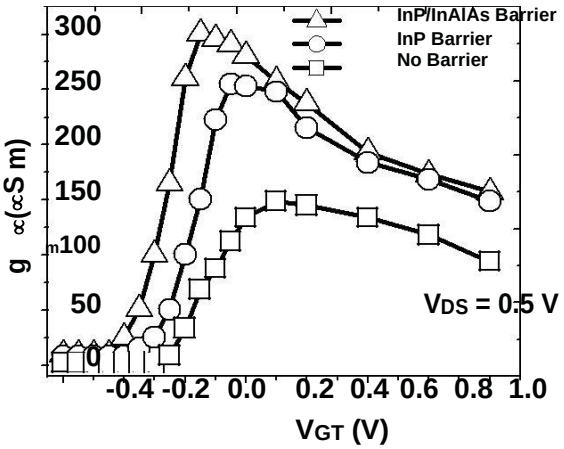
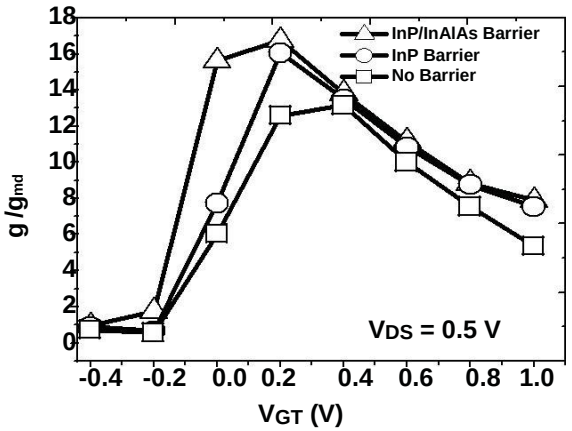


Fig. 3. Comparison of g_m at V_{DS} = 0.5 V as a function of gate overdrive voltage V_{GT} for the three types of $In_{0.7}Ga_{0.3}As$ MOSFETs.

is, however, nominal [3] that in turn reduces g_m marginally. Furthermore, as the gate voltage increases, the centroid of the inversion charge density in the channel is pulled toward the Al_2O_3 interface in the Al_2O_3/barrier/$In_x Ga_{1-x}$ As structure. This phenomenon increases scattering due to interface-trapped charges thereby reducing the carrier mobility, as explained in [3]. Consequently, g_m degrades at a much higher rate with

increasing V_{GS} for such devices. The g_m /I_{DS} is an important device parameter for analog circuit performance, since g_m represents the amplification delivered by the device and I_{DS} represents the power dissipation to obtain the amplification. Therefore, higher the g_m /I_{DS} ratio, more suitable is the device for analog applications. Fig. 4 shows a comparison of g_m /I_{DS} as a function of V_{GT} between three different devices. It is observed in Fig. 4 that, although a single-barrier device shows marginal improvement in g_m /$I_{D\,S}$, the same is significant for a double-barrier device. A comparison of g_d as a function of V_{GT} between the above three devices is shown in Fig. 5. It is observed in Fig. 5 that the device with no barrier shows the smallest value of g_d as compared with the devices with a single barrier or a double barrier. The value of g_d for a typical long-channel device, which shows perfect output current saturation, is very low (ideally zero). The value of g_d increases with device scaling due to the SCEs, such as channel length modulation and DIBL. The gate control over the channel increases as one moves from the double-barrier device to the no barrier device through the single-barrier device. The impact of SCEs, such as DIBL, is also reduced accordingly, thereby reducing the value of g_d . A decrease in g_d is expected by adopting SCE reduction techniques such as use of a dual-material gate in the device [17], [18]. Fig. 6 shows a comparison of the intrinsic voltage gain g_m /g_d as a function of



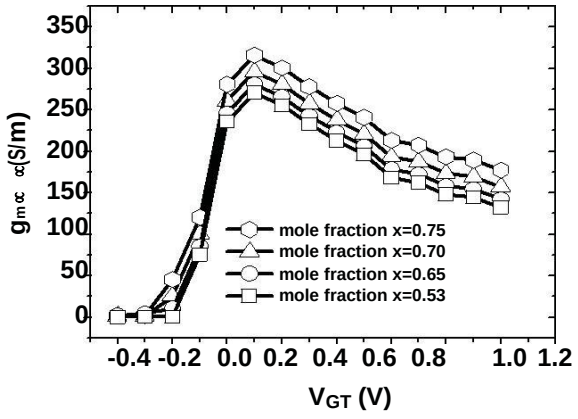


Fig. 6. Comparison of intrinsic voltage gain g_m /g_d at V_{DS} = 0.5 V as a function of V_{GT} for the three types of $In_{0.7}Ga_{0.3}As$ MOSFETs.

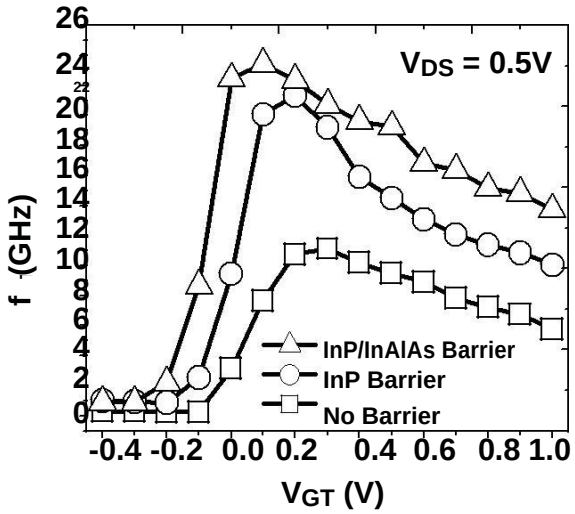


Fig. 7. Comparison of unity-gain cut-off frequency fT at VDS = 0.5 V as a function of VGT for the three types of $In_{0.7}Ga_{0.3}As$ MOSFETs.

VGT between the three different device structures. It is evident in Fig. 6 that a barrier layer helps improve the device gain, with a double-barrier layer producing the highest gain. This is due to the significant improvement in gm when a barrier layer is used in the device, as observed in Fig. 3, in spite of the fact that the improvement in gm is partially compensated by the higher value of gd , as observed in Fig. 5. Fig. 7 shows a comparison of fT as a function of VGT between the three different device structures. The device with a double-barrier layer exhibits the highest value of fT as compared with other devices, which is again due the improvement in gm for such devices.

Fig. 8. Comparison of gm at VDS = 0.5 V as a function of VGT for different mole fractions of indium in InGaAs MOSFET with a double-barrier layer.

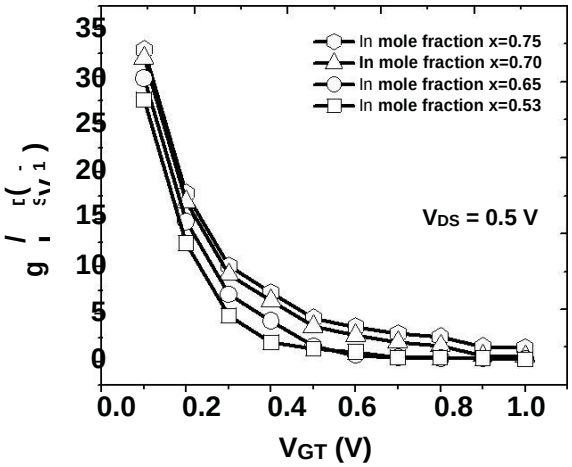
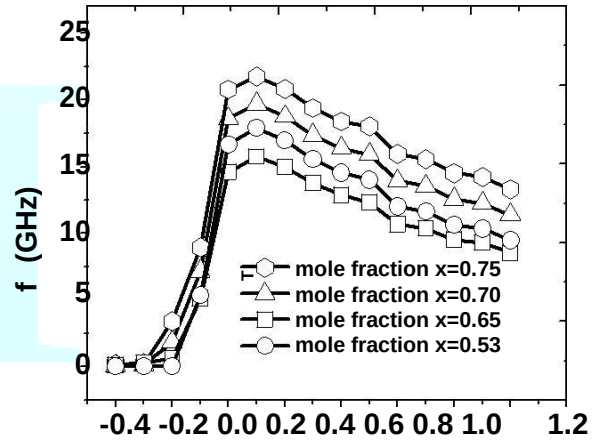


Fig. 9. Comparison of gm / ID at VDS = 0.5 V as a function of gate overdrive voltage VGT for different mole fractions of indium in InGaAs MOSFET with a double-barrier layer.



B. Effect of Indium Content

We now investigate the impact of varying the mole fraction of indium in the channel of an InGaAs MOSFET on its analog performance. As an InGaAs MOSFET with a double-barrier layer produces the best performance for analog applications, as found in Section III-A, we use such a device for this investigation. Fig. 8 shows the variation of g_m as a function of V_{GT} at V_{DS} = 0.5 V for varying mole fraction of indium in

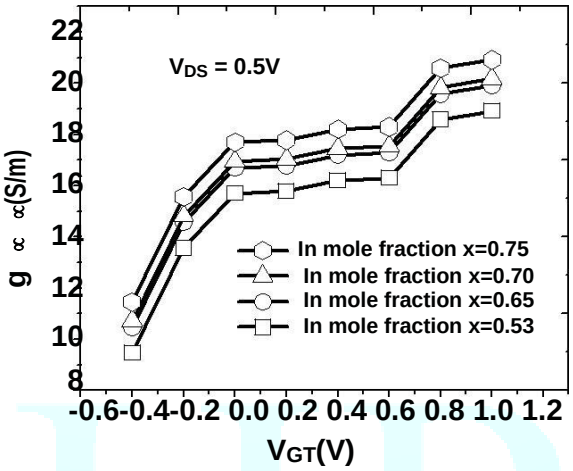


Fig. 11. Comparison of g_d as a function of gate overdrive voltage V_{GT} for different mole fractions of indium in InGaAs MOSFET with a double-barrier layer.

an In molar fraction of 0.53 is 5.86A°, which matches well with that of $In_{0.52}Al_{0.48}As$. For an In molar fraction below 0.53, the lattice constant of InGaAs becomes smaller than that of $In_{0.52}Al_{0.48}As$ resulting in a tensile strain in the InGaAs layer. On the other hand, for an In molar fraction exceeding 0.53, the lattice constant of the InGaAs layer becomes larger than 5.86A° and the channel is subjected to a compressive strain. The impact of alloy scattering on the electron mobility was discussed in detail in [19]. As the compressive strain increases, the alloy scattering decreases, resulting in improved electron mobility. Most importantly, a large indium content in the channel material enhances the electron mobility in the channel [3], [4], [11]–[13], and also increases the conduction band offset between the channel and barrier layer, as shown in Table I, resulting in improved carrier confinement. Both effects facilitate improvement in drain current I_{DS} [20], and also in g_m , as evident in Fig. 8. Fig. 9 shows a comparison of g_m /I_{DS} as the function of V_{GT} for the above-mentioned device with four different values of indium mole fractions. It is observed in Fig. 9 that g_m /I DS increases for increasing indium mole fraction. Fig. 10 shows a comparison of fT as a function of V_{GT} for different values of indium mole fraction in the channel. It is evident in Fig. 10 that fT also increases for increasing indium mole fraction in the channel, which is again due to the improvement in g_m for increasing indium mole fraction, as

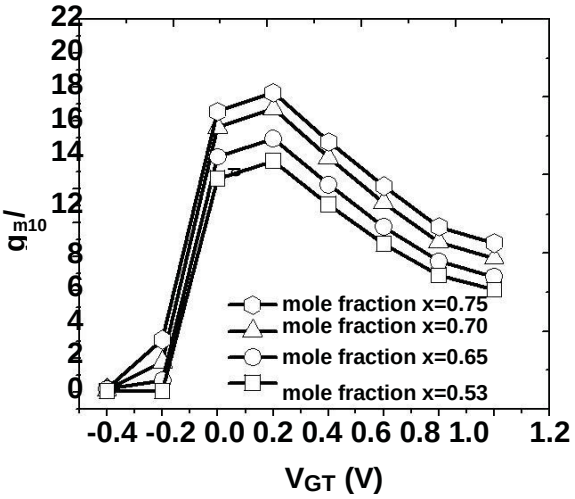


Fig. 12. Comparison of device gain g_m /g_d at V_{DS} = 0.5 V as a function of gate overdrive voltage V_{GT} for different mole fractions of indium in InGaAs MOSFET with a double-barrier layer.

observed in Fig. 8. A comparison of g_d as a function of V_{GT} for different values of indium mole fraction in the channel is shown in Fig. 11. It is observed in Fig. 11 that InGaAs channel with a larger amount of indium mole fraction in it exhibits a larger value of g_d . As the In content is increased, the dielectric constant of the channel material is also increased, which in turn increases the junction capacitances. As a result, SCEs become more pronounced due to larger charge sharing between the source and the drain thereby increasing g_d . Fig. 12 shows a comparison of the intrinsic voltage gain g_m /g_d as a function of V_{GT} between the device structures with different values of indium mole fraction. It is evident in Fig. 12 that the device with a larger mole fraction of indium in the channel results in higher device gain. This is due to the significant improvement in g_m for increasing mole fraction of indium in the channel, as observed in Fig. 8, in spite of the fact that the improvement in g_m is partially compensated by the higher value of g_d , as observed in Fig. 11.

IV. Conclusion

A detailed investigation on the influence of a barrier layer as well as the indium content in the channel on the analog circuit performance of InGaAs MOSFETs was made. It was found that, although a barrier layer improves the analog performance parameters, except g_d , of the device in general, the improvement is significant for the

device with a double-barrier layer. A higher indium content in the channel of such a device was also found to improve its analog performance parameters in general, except g_d . A higher indium content increases the output conductance due to the higher value of dielectric constant. Further improvement in the analog circuit performance of an InGaAs MOSFET with a double-barrier layer and higher indium content may be possible by improving g_d with the use of some SCE reduction techniques.

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